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| EXAMINER | |
|---|---|
| MANOSKEY, JOSEPH D | |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/805,182 | MICHELONI ET AL. | |
| | Examiner | Art Unit | |
| | JOSEPH D. MANOSKEY | 2113 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *11 August 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 5, 9, 10, 12-17, and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pittelkow et al., U.S. Patent 6,966,741, hereinafter referred to as "Pittelkow" in view of Chow et al., U.S. Patent App. Pub. 2002/0069317, hereinafter referred to as "Chow".

3. As per claim 1, Pittelkow discloses:

An integrated memory system (See Pittelkow, figure 2: controller 201), comprising at least a non-volatile memory (See Pittelkow, figure 2: NVRAM 228 is non volatile, and interfaces 222a-222c lead to disk storage, which is nonvolatile; column 8 lines 36-43: configuration control board 202 may also contain NVRAM), and an automatic storage error corrector (See Pittelkow, column 9 lines 36-43), including functionally independent devices (See Pittelkow, figure 5: multiple independent configuration circuit boards may be used), each device to correct a different

predetermined storage error (See Pittelkow, column 25: table lists predetermined error types, including single bit error correction code errors),

at least one of said devices being external to the memory (See Pittelkow, column 9 lines 36-40: the CCB may send the failure to another failure manager which may be in another controller. The limitation: "external to the memory" is taken to mean: "external to the non-volatile memory," as opposed to "external to the memory system").

Pittelkow does not teach the a “predetermined storage error of data stored in the memory” wherein the memory is “a non-volatile solid-state memory”. However Pittelkow does teach of the use of NVRAM and disk storage (See figure 2). Chow teaches the use of solid-state drives, SSDs (See Chow paragraph 0010). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine SSDs of Chow with the system of Pittelkow, because the SSDs are faster than disk drives (See Chow paragraph 0010).

4. As per claim 2, Pittelkow and Chow disclose:

A system according to claim 1, wherein said memory is connected to a controller by means of an interface bus (See Pittelkow, column 8 lines 36-43: configuration control board 202 may contain NVRAM: this would require a bus for access. Figure 2: NVRAM is accessed by front and back end processors, which are connected to CCB by busses 214 and 218. Disk storage is connected by bus 226 (See Pittelkow, figure 2)).

and said devices are incorporated both in the memory and in the controller (See Pittelkow, figure 2: configuration control board is incorporated With the nonvolatile memories).

5. As per claim 5, Pittelkow and Chow disclose:

A system according to claim 2, including a circuit to generate a signal to request the external correction of an error by said controller (See Pittelkow, column 9 lines 36-40: the CCB may send the failure to another failure manager, which may be in another controller).

6. As per claim 9, Pittelkow discloses:

A system, comprising:

a first circuit operable to store data having associated therewith at least one storage error of a plurality of storage-error types the first circuit operable to correct a first-type error of the plurality of storage-error types (See Pittelkow, figures 2 and 3, and column 9 lines 36-40: storage controller 201 contains failure manager 302, which is capable of detecting and correcting errors such as those listed in the table of column 25); and

a second circuit coupled to the first circuit (See Pittelkow, figure 5: multiple storage controllers may be used and coupled),

the second circuit operable to correct a second-type error of the plurality of storage-error types (See Pittelkow, figures 2 and 3: storage controller 201 contains

failure manager 302, which is capable of detecting the types of errors listed in the table of column 25, including single bit error correction code errors).

Pittelkow does not teach the a "in a non-volatile solid-state memory". However Pittelkow does teach of the use of NVRAM and disk storage (See figure 2). Chow teaches the use of solid-state drives, SSDs (See Chow paragraph 0010). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine SSDs of Chow with the system of Pittelkow, because the SSDs are faster than disk drives (See Chow paragraph 0010).

7. As per claim 10, Pittelkow and Chow disclose:

The system of claim 9 wherein the second circuit to generate a signal requesting correction of a third-type error of the plurality of storage-error types (See Pittelkow, column 25: several different error types can be detected. Column 9 lines 36-40: the CCB may send the failure to another failure manager which may be in another controller. Column 4 lines 9-13: a master and one or more slave controllers may be used).

8. As per claim 12, Pittelkow and Chow disclose:

The system of claim 9 wherein the first circuit further to detect the second-type error (See Pittelkow, figures 2 and 3: storage controller 201 contains failure manager 302, which is capable of detecting any of the types of errors listed in the table of column 25).

9. As per claim 13, Pittelkow and Chow disclose:

The system of claim 9 wherein the second circuit to correct the second-type error in response to a signal generated by the first circuit (See Pittelkow, column 9 lines 36-40: the CCB may send the failure to another failure manager which handles the error).

10. As per claim 14, Pittelkow and Chow disclose:

The system of claim 9 wherein the first circuit comprises a non-volatile memory (See Pittelkow, figure 2: NVRAM 228 is non volatile, and interface 22a-222c lead to disk storage, which is nonvolatile; column 8 lines 36-43: configuration control board 202 may also contain NVRAM).

11. As per claim 15, Pittelkow and Chow disclose:

The system of claim 9 wherein: the first circuit is disposed on a first integrated circuit; and the second circuit is disposed on a second integrated circuit.

Pittelkow discloses that his storage controller comprises a plurality of processors, interpreted as “integrated circuits”, a configuration and control board, and storage means (column 7 lines 39-47). Pittelkow also discloses that the controllers may be separate and connected by a network (figure 5: controller 1 and controller 2 are connected by administrative network 520).

12. As per claim 16, Pittelkow and Chow disclose:

The system of claim 9 wherein the first and second circuits are disposed on an integrated circuit.

Pittelkow discloses that his storage controller comprises a plurality of processors, interpreted as "integrated circuits", a configuration and control board, and storage means (column 7 lines 39-47).

13. As per claim 17, Pittelkow discloses:

A memory device, comprising:

a storage portion to store data having associated therewith at least one storage error of a plurality of storage-error types (See Pittelkow, column 8 lines 48-53: the CCB is associated with RAID devices, and may perform failure notification and diagnostics on' the RAID devices);

a first circuit to correct a first-type error of the plurality of storage-error types (See Pittelkow, figures 2 and 3, and column 9 lines 36-40: storage controller 201 contains failure manager 302, which is capable of detecting and correcting errors such as those listed in the table of column 25, including single bit error correction code errors); and

a second circuit to generate a signal indicating detection of a second- type error of the plurality of storage-error types (See Pittelkow, figure 5: multiple independent configuration circuit boards may be used).

Pittelkow does not teach the a "non-volatile solid-state storage". However Pittelkow does teach of the use of NVRAM and disk storage (See figure 2). Chow teaches the use of solid-state drives, SSDs (See Chow paragraph 0010). It would have

been obvious to one of ordinary skill in the art at the time of the invention to combine SSDs of Chow with the system of Pittelkow, because the SSDs are faster than disk drives (See Chow paragraph 0010).

14. As per claim 19, Pittelkow discloses:

A method, comprising:

storing, in a memory location of a device, data having associated therewith at least one storage error of a plurality of storage-error (See Pittelkow, figures 2 and 3, and column 9 lines 36-40: storage controller 201 contains failure manager 302, which is capable of detecting and correcting errors such as those listed in the table of column 25); and correcting, at the memory location, a first-type error of the plurality of storage-error types (See Pittelkow, figures 2 and 3, and column 9 lines 36-40: storage controller 201 contains failure manager 302, which is capable of detecting and correcting errors such as those listed in the table of column 25, including single bit error correction code errors).

Pittelkow does not teach the a "non-volatile solid-state memory". However Pittelkow does teach of the use of NVRAM and disk storage (See figure 2). Chow teaches the use of solid-state drives, SSDs (See Chow paragraph 0010). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine SSDs of Chow with the system of Pittelkow, because the SSDs are faster than disk drives (See Chow paragraph 0010).

15. As per claim 20, Pittelkow and Chow disclose:

The method of claim 19, further comprising generating, at the memory location, an interrupt-request signal indicating detection of a second-type error of the plurality of storage-error types (See Pittelkow, column 9 lines 36-40).

16. As per claim 21, Pittelkow discloses:

An electronic system, comprising:

a first integrated circuit having a memory to store data having associated therewith at least one storage error of a plurality of storage-error types, the memory to correct a first-type error of the plurality of storage-error types (See Pittelkow, figures 2 and 3, and column 9 lines 36-40: storage controller 201 contains failure manager 302, which is capable of detecting and correcting errors such as those listed in the table of column 25, including single bit error correction code errors); and

a second integrated circuit coupled to the first circuit, the second integrated circuit having processor to correct a second-type error of the plurality of storage-error types (See Pittelkow, figure 5: multiple independent configuration circuit boards may be used. Column 8 lines 36-43: this may include a processor).

Pittelkow does not teach the a "non-volatile solid-state memory". However Pittelkow does teach of the use of NVRAM and disk storage (See figure 2). Chow teaches the use of solid-state drives, SSDs (See Chow paragraph 0010). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine

SSDs of Chow with the system of Pittelkow, because the SSDs are faster than disk drives (See Chow paragraph 0010).

17. Claims 3, 4, 6-8, 11, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pittelkow and Chow in view of Saxena et al., U.S. Patent 5,533,035, hereinafter referred to as “Saxena”.

18. As per claim 3, Pittelkow and Chow do not disclose:

A system according to claim 1, including coding to correct two errors, a logic to calculate a syndrome, a single error correcting circuit, and a logic to detect more than one error.

Saxena discloses a system (figure 5) that reads data having error-correction code from a memory (column 10 lines 21-28), calculates a syndrome for the data (column 10 lines 35-42), and, using the syndrome, corrects a single bit error, (column 10 lines 53-56), or a double bit error (column 10 lines 56-60). Pittelkow discloses that an error correction code may be used (column 25 lines 30-34: "Single Bit Error Correction Code Error"), and that other types of errors may also be corrected in the failure manager(column 26 lines 20-27). An error correction code capable of correcting more than one error in a dataset would enable the system to correct multiple errors instead of just one. This would be an obvious benefit in retaining reliability of storage systems, because data with more than 1 bit error would not be lost. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate error

correction capabilities and syndrome calculation into the system of Pittelkow and Chow, increasing reliability.

19. As per claim 4, Pittelkow and Chow do not disclose:

A system according to claim 3, further including a logic to supply the controller with a one-no-error-corrected data, the uncorrected error, and the calculated syndrome.

Saxena discloses a system (figure 5) that reads data having error-correction code from a memory (column 10 lines 21-28), calculates a syndrome for the data (column 10 lines 35-42), and, using the syndrome, corrects a single bit error, (column 10 lines 53-56), or a double bit error (column 10 lines 56-60). These steps are executed in an error correction unit (column 10 lines 21-25). Pittelkow discloses that an error correction code may be used (column 25 lines 30-34: "Single Bit Error Correction Code Error"), and that other types of errors may also be corrected in the failure manager (column 26 lines 20-27). An error correction code capable of correcting more than one error in a dataset would enable the system to correct multiple errors instead of just one. This would be an obvious benefit in retaining reliability of storage systems, because data with more than 1 bit error would not be lost. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate error correction capabilities and syndrome calculation into the system of Pittelkow and Chow, increasing reliability.

20. As per claim 6, Pittelkow discloses:

A system according to claim 3, wherein said coding block is located immediately downstream of the input terminal of said memory to perform a vector product proportional to the number of parity bits and obtained through the synthesis of a corresponding logic function.

Saxena discloses a system (figure 5) that reads data having error-correction code from a memory (column 10 lines 21-28), calculates a syndrome for the data (column 10 lines 35-42), and, using the syndrome, corrects a single bit error, (column 10 lines 53-56), or a double bit error (column 10 lines 56-60). The error correction code is calculated by the synthesis of a series of logic functions (column 7 lines 20-29). These steps are performed by error code generator 30, immediately downstream of the an input terminal (column 5 lines 38-40 and figure 1). Pittelkow discloses that an error correction code may be used (column 25 lines 30-34: "Single Bit Error Correction Code Error"), and that other types of errors may also be corrected in the failure manager (column 26 lines 20-27). An error correction code capable of correcting more than one error in a dataset would enable the system to correct multiple errors instead of just one. This would be an obvious benefit in retaining reliability of storage systems, because data with more than 1 bit error would not be lost. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate error correction capabilities and syndrome calculation into the system of Pittelkow and Chow, increasing reliability.

21. As per claim 7, Saxena discloses:

A system according to claim 6, wherein said logic to calculate the syndrome to use a parity calculation circuit of the coding circuit.

Saxena discloses a system (figure 5) that reads data having error-correction code from a memory (column 10 lines 21-28), calculates a syndrome for the data (column 10 lines 35-42), and, using the syndrome, corrects a single bit error, (column 10 lines 53-56), or a double bit error (column 10 lines 56-60). The error correction code is calculated by error code generator 30 (column 5 lines 38-40 and figure 1). Pittelkow discloses that an error correction code may be used (column 25 lines 30-34: "Single Bit Error Correction Code Error"), and that other types of errors may also be corrected in the failure manager (column 26 lines 20-27). An error correction code capable of correcting more than one error in a dataset would enable the system to correct multiple errors instead of just one. This would be an obvious benefit in retaining reliability of storage systems, because data with more than 1 bit error would not be lost. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate error correction capabilities and syndrome calculation into the system of Pittelkow and Chow, increasing reliability.

22. As per claim 8, Pittelkow discloses:

A system according to claim 3, wherein said single error correcting circuit an error comprises a block to decode a single error effective to recognize each of the several syndromes associated to a single error to activate, through a corresponding vector, the correction of the corresponding bit.

Saxena discloses a system (figure 5) that reads data having error-correction code from a memory (column 10 lines 21-28), calculates a syndrome for the data (column 10 lines 35-42); and, using the syndrome, corrects a single bit error, (column 10 lines 53-56), or a double bit error (column 10 lines 56-60). Pittelkow discloses that an error correction code may be used (column 25 lines 30-34: "Single Bit Error Correction Code Error"), and that other types of errors may also be corrected in the failure manager (column 26 lines 20-27). An error correction code capable of correcting more than one error in a dataset would enable the system to correct multiple errors instead of just one. This would be an obvious benefit in retaining reliability of storage systems, because data with more than 1 bit error would not be lost. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate error correction capabilities and syndrome calculation into the system of Pittelkow and Chow, increasing reliability.

23. As per claim 11, Pittelkow discloses:

The system of claim 9 wherein the first circuit further to determine at least one syndrome associated with the at least one storage error.

Saxena discloses a system (figure 5) that reads data having error-correction code from a memory (column 10 lines 21-28), calculates a syndrome for the data (column 10 lines 35-42), and, using the syndrome, corrects a single bit error, (column 10 lines 53-56), or a double bit error (column 10 lines 56-60). Pittelkow discloses that an error correction code may be used (column 25 lines 30-34: "Single Bit Error Correction

Code Error"), and that other types of errors may also be corrected in the failure manager (column 26 lines 20-27). An error correction code capable of correcting more than one error in a dataset would enable the system to correct multiple errors instead of just one. This would be an obvious benefit in retaining reliability of storage systems, because data with more than 1 bit error would not be lost. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate error correction capabilities and syndrome calculation into the system of Pittelkow and Chow, increasing reliability.

24. As per claim 18, Pittelkow does not disclose:

The device of claim 17, further comprising a third circuit to determine at least one syndrome associated with the at least one storage error.

Saxena discloses a system (figure 5) that reads data having error-correction code from a memory (column 10 lines 21-28), calculates a syndrome for the data (column 10 lines 35-42), and, using the syndrome, corrects a single bit error, (column 10 lines 53-56), or a double bit error (column 10 lines 56-60). Pittelkow discloses that an error correction code may be used (column 25 lines 30-34: "Single Bit Error Correction Code Error"), and that other types of errors may also be corrected in the failure manager portion of the controller (column 26 lines 20-27). Pittelkow also discloses that any number of controllers may be used (column 4 lines 9-13: a master and one or more slave controllers). A syndrome calculator would enable the controller to find and correct one or more errors in the ECC data. This would have the obvious benefit of improving

reliability of storage systems, because data with more than 1 bit error would be correctable. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate syndrome calculation into the system of Pittelkow and Chow, increasing reliability.

### *Response to Arguments*

27. Applicant's arguments filed 11 August 2008 have been fully considered but they are not persuasive. The Applicant argues that Pittelkow does not teach using functionally independent devices, each of which corrects a different storage error. The Examiner respectfully disagrees. Pittelkow teaches the failure manager, if unable to handle the error, forwarding it to another failure manger in another controller that can handle the failure (See Col. 9, lines 36-43). One can not handle the error and one can, therefore correcting different errors. They are in different controllers, therefore functionally independent, with one in the system and one external.

### *Conclusion*

28. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOSEPH D. MANOSKEY whose telephone number is (571)272-3648. The examiner can normally be reached on Mon.-Fri. (7:30am to 4pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JDM

December 4, 2008

/Robert W. Beausoliel, Jr./
Supervisory Patent Examiner, Art Unit 2113